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Description

METHOD FOR FABRICATING A DEEP TRENCH CAPACITOR

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a semiconductor process, and more particularly, to a process of manufacturing a deep trench capacitor of a DRAM device.

[0003] 2. Description of the Prior Art

[0004] Trench-capacitor DRAM devices are known in the art. A trench-storage capacitor typically consists of a very-high-aspect-ratio contact-style hole pattern etched into the substrate, a thin storage-node dielectric insulator, a doped low-pressure chemical vapor deposition (LPCVD) polysilicon fill, and buried-plate diffusion in the substrate. The doped LPCVD silicon fill and the buried plate serve as the electrodes of the capacitor. A dielectric isolation collar in the upper region of the trench prevents leakage of the

signal charge from the storage-node diffusion to the buried-plate diffusion of the capacitor.

[0005] In general, the prior art method for fabricating a trench capacitor of a DRAM device may include several major manufacture phases as follows:

[0006] Phase 1: deep trench etching.

[0007] Phase 2: buried plate and capacitor dielectric (or node dielectric) forming.

[0008] Phase 3: first polysilicon deep trench fill and first recess etching.

[0009] Phase 4: collar oxide forming.

[0010] Phase 5: second polysilicon deposition and second recess etching.

[0011] Phase 6: third polysilicon deposition and third recess etching.

[0012] Phase 7: shallow trench isolation (hereinafter referred to as "STI") forming.

[0013] Please refer to Fig.1 to Fig.3. Fig.1 is a schematic diagram illustrating an enlarged portion of a typical deep trench capacitor in cross-sectional view along line NN' of Fig.2. Fig.2 shows the normal layout of the active areas (hereinafter referred to as "AA") and deep trench capaci-

tors (hereinafter also referred to as "DT") 11 and 12 without DT-AA misalignment after accomplishing STI process, wherein perspective buried strap out diffusion 16 is shown. Fig.3 depicts misaligned AA and DT layout after accomplishing STI process. Referring initially to Fig.1, two adjacent deep trench capacitors (DT) 11 and 12 are fabricated in a semiconductor substrate 10, wherein each of which is comprised of a buried plate 13, node dielectric 14, poly stack storage node (Poly1/Poly2/Poly3). As known to those skilled in the art, the buried plate 13 acts as a first electrode of the deep trench capacitor, and the poly stack storage node (Poly1/Poly2/Poly3), which is electrically isolated from the buried plate 13 by the node dielectric 14, acts as a second electrode of the deep trench capacitor. Typically, the second polysilicon layer (Poly2) of the poly stack storage node (Poly1/Poly2/Poly3) is electrically from the surrounding substrate 10 by a so-called collar oxide 15. The deep trench capacitors 11 and 12 are electrically connected to respective access transistors (not shown), which are formed on the active areas 26, via the buried strap out diffusions 16. The deep trench capacitor 11 is electrically isolated from the deep trench capacitor 12 by the STI 20.

[0014] As the size of a memory cell shrinks, the chip area available for a single memory cell becomes very small. This causes reduction in capacitor area on a single chip and therefore leads to problems such as inadequate capacitance and large electrode resistance. In Fig.1, two essential parameters are defined: X and L, wherein the parameter "X" stands for the maximum distance in the overlapping region between AA and DT in the x-direction, and the parameter "L" stands for the maximum distance of the DT in the x-direction subtracts the parameter "X". In other words, the maximum width of the DT in the x-direction is the combination of the parameters "X" and "L". It is often desired that to minimize the electrode resistance, the parameter "L" is kept as small as possible, while the parameter "X" is kept as large as possible. Larger "X" means longer AA region, and smaller "L" means narrower STI between two adjacent deep trench capacitors. Referring to Fig.3, unfortunately, small "L" often leads to AA-DT misalignment when defining AA and STI areas, and therefore causes capacitor charge leakage via diffusion region 17 as shown in dash line circle. When AA-DT misalignment occurs, the conductive diffusion region 17 is formed in the area between two adjacent deep trench capacitors 11 and

12, in which a STI is supposed to embedded therein for isolating the two adjacent deep trench capacitors 11 and 12.

[0015] Please refer to Fig.4 and Fig.5. Fig.4 and Fig.5 are schematic cross-sectional diagrams showing several intermediate steps of forming a prior art deep trench capacitor, which are relative to the present invention. As shown in Fig.4, a substrate 10 having a pad oxide layer 26 and a pad nitride layer 28 thereon is provided. After deep trench etching, an N^+ buried plate 13 and a node dielectric layer 14 are sequentially formed in the deep trench. A first polysilicon deposition and recess process is then carried out to form a first poly layer (Poly1) at the bottom of the deep trench. A collar oxide layer 15 is formed on sidewall of the deep trench above Poly1. A second polysilicon deposition and recess process is then carried out to form a second poly layer (Poly2) atop Poly1. As shown in Fig.5, the collar oxide layer 15 that is not covered by Poly 2 is stripped off to expose the sidewall of the deep trench. Subsequently, a third polysilicon deposition and recess process is carried out to form a third poly layer (Poly3) atop Poly2. Dopants of the heavily doped Poly2 diffuse out through Poly3 to the surrounding substrate 10 to form an

annular shaped buried strap out diffusion 16. Finally, a conventional STI process is performed to isolate the two adjacent deep trench capacitors, thereby forming the structure as set forth in Fig.1.

SUMMARY OF INVENTION

[0016] The primary objective of the present invention is to provide a novel method for fabricating a trench capacitor of DRAM devices, thereby solving prior art AA-DT misalignment problem during STI process and reducing resistance of the capacitor electrode.

[0017] According to the claimed invention, a method for fabricating a trench capacitor is disclosed. A substrate having thereon a pad oxide layer and a pad nitride layer is provided. A deep trench is formed by etching the pad nitride layer, the pad oxide layer, and the substrate. The deep trench is then doped to form a buried diffusion plate in the substrate at a lower portion of the deep trench. A node dielectric layer is deposited in the deep trench. A first polysilicon deposition and recess etching is performed to embed a first polysilicon layer on the node dielectric layer at the lower portion of the deep trench, and the first polysilicon layer having a top surface, wherein the d top surface of the first polysilicon layer and sidewall of

the deep trench define a first recess. A collar oxide layer is formed on sidewall of the first recess. A second polysilicon deposition and recess etching is performed to embed a second polysilicon layer on the first polysilicon layer. A mask layer is form to partially mask the collar oxide layer. The collar oxide layer that is not masked by the mask layer and the second polysilicon (Poly2) layer is then stripped off. The mask layer is removed. A third polysilicon deposition and recess etching is then carried out to embed a third polysilicon (Poly3) layer on the second polysilicon (Poly2) layer.

[0018] It is to be understood that both the foregoing general description and the following detailed description are exemplary, but are not restrictive, of the invention. Other objects, advantages, and novel features of the claimed invention will become more clearly and readily apparent from the following detailed description when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF DRAWINGS

[0019] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, to-

gether with the description, serve to explain the principles of the invention. In the drawings:

[0020] Fig.1 is a schematic diagram illustrating an enlarged portion of a typical deep trench capacitor in cross-sectional view along line NN' of Fig.2;

[0021] Fig.2 shows the normal AA and DT layout without DT-AA misalignment after accomplishing STI process, wherein perspective buried strap out diffusion 16 is shown;

[0022] Fig.3 depicts misaligned AA and DT layout after accomplishing STI process, wherein perspective buried strap out diffusion 16 and excess conductive diffusion 17 are shown;

[0023] Fig.4 and Fig.5 are schematic cross-sectional diagrams showing several intermediate steps of forming a prior art deep trench capacitor;

[0024] Fig.6 to Fig.9 are schematic cross-sectional diagrams showing the manufacture steps of making a deep trench capacitor in accordance with the first preferred embodiment of the present invention;

[0025] Fig.10 is a top view of Fig.9 in a state before STI etching process, wherein the perspective non-annular buried strap out diffusion and single-sided spacer are illustrated;

[0026] Fig.11 is a top view layout in a DT-AA misaligned state

before STI etching process in accordance with the second preferred embodiment of the present invention; and

[0027] Fig.12 is a top view layout before STI etching process in accordance with the third preferred embodiment of the present invention.

DETAILED DESCRIPTION

[0028] Please refer to Fig.6 to Fig.9. Fig.6 to Fig.9 are schematic cross-sectional diagrams showing the manufacture steps of making a deep trench capacitor in accordance with the first preferred embodiment of the present invention, in which like reference numerals designate similar or corresponding elements, regions, and portions. As shown in Fig.6, a semiconductor substrate 10 such as a silicon substrate is provided. A pad oxide layer 26 and a pad nitride layer 28 are formed on a main surface of the semiconductor substrate 10. A dry etching process is carried out to form a deep trench in the semiconductor substrate 10. A buried plate 13 adjacent to the deep trench and a node dielectric layer 14 are formed. A first polysilicon deposition and recess process is carried out to form a first poly layer (Poly1) at the bottom of the deep trench. A collar oxide layer 15 is formed on sidewall of the deep trench above Poly1. A second polysilicon deposition and recess

process is then carried out to form a second poly layer (Poly2) atop Poly1. The method of forming the buried plate 13 comprises the steps of depositing a thin layer of arsenic silicate glass (ASG) at a lower portion of the deep trench, followed by thermal drive in. It is understood that other doping methods such as gas phase doping (GPD) or the like may be employed. The node dielectric layer 14 may be oxide-nitride (ON) or oxide-nitride-oxide (ONO), but not limited thereto. After performing the second polysilicon deposition and recess process, the top surface of Poly2 and the surface of the collar oxide layer 15 define a recess 32 at the top of the deep trench.

[0029] As shown in Fig.7, the recess 32 is filled with a sacrificial layer 34. The sacrificial layer 34 is also deposited on the pad nitride layer 28. According to the preferred embodiment of this invention, the sacrificial layer 34 is an anti-reflection coating (ARC) material typically used in semiconductor processes. Thereafter, a lithographic process is carried out to form a photoresist layer 36 on the sacrificial layer 34. The photoresist layer 36 partially masks the underlying sacrificial layer 34 that is deposited within the recess 32 and partially overlaps with the collar oxide layer 15.

[0030] As shown in Fig.8, using the photoresist layer 36 and the pad nitride layer 28 as an etching mask, an anisotropic dry etching process is performed to etch the sacrificial layer 34 and the collar oxide layer 15 that are not covered by the photoresist layer 36. Asymmetric collar oxide structure is thus formed. A portion of the collar oxide layer 15, which is protected by the photoresist layer 36 during the dry etching, remains intact and forms a single-sided spacer 42 in the recess 32. The collar oxide layer 15 that is not protected by the photoresist layer 36 is etched away to a surface that is lower than the exposed top surface of Poly2. As seen in Fig.8, the asymmetric collar oxide structure includes an annular lower portion, which encircles Poly2 and isolates Poly2 from the substrate 10, and the upper portion, i.e., the single-sided spacer 42, which blocks the path through which dopants of Poly2 out diffuse, via a Poly3 layer (not yet formed at this stage) atop the Poly2, to the substrate 10. Next, the photoresist layer 36 and the sacrificial layer 34 are removed by methods known in the art, thereby forming a recess 57, which is substantially defined by the surface of the single-sided spacer 42, the top surface of Poly2, and the exposed sidewall substrate 10 above the collar oxide layer 15.

[0031] As shown in Fig.9, a third polysilicon deposition and recess etching process is carried out to form a third polysilicon layer (Poly3) atop Poly2. First, a CVD polysilicon layer (not shown) is deposited over the substrate 10 and fills the recess opening 57. The CVD polysilicon layer is then recessed to a predetermined depth, for example, a depth of about 100~500 angstroms below the surface of the semiconductor substrate 10. It is to be understood that the surface of the semiconductor substrate 10 means the interface between the pad oxide layer 26 and the bulk substrate 10. Dopants of the heavily doped Poly2 diffuse out through Poly3 to the surrounding substrate 10 that is not masked by the single-sided spacer 42 to form a non-annular buried strap out diffusion 62, which connects a source region of an access transistor (not shown and not yet formed at this stage) with the storage node of the trench capacitor. Finally, an STI process, which is known in the art, is carried out. By way of example, a borosilicate glass (BSG) layer is deposited over the substrate 10 and fills the recess opening above Poly3 in the trench. An AA photoresist is formed on the BSG layer to define the active areas. The AA photoresist has therein an STI opening defining the STI region to be etched into the substrate 10.

[0032] Please refer to Fig.10. Fig.10 is a top view of Fig.9 in a state after forming AA photoresist 70 but before STI etching process, wherein the perspective non-annular buried strap out diffusion 62 and single-sided spacer 42 are illustrated. It is shown that due to the existence of the single-sided spacer 42, the STI opening width between two adjacent deep trenches can be very small without the fear of AA-DT misalignment. It is noted that smaller STI opening width between two adjacent deep trenches means longer active area pattern (defined by the AA photoresist 70), as shown in Fig.10. Buried strap out diffusion 62 only forms through the sidewall that is not blocked by the single-sided spacer 42 that is situated adjacent to a neighboring deep trench capacitor. Therefore, there is substantially no out diffusion region between two adjacent trench capacitors. The extended AA has a modified parameter X'(the maximum distance in the overlapping region between AA and DT in the x-direction) that is larger than the prior art parameter X, and a modified parameter L' (the maximum distance of the DT in the x-direction subtracts the parameter X') that is smaller than the prior art parameter L.

[0033] Please refer to Fig.11. Fig.11 is a top view layout in a DT-

AA misaligned state after forming the AA photoresist 80 but before STI etching process in accordance with the second preferred embodiment of the present invention. As shown in Fig.11, buried strap out diffusion 62 only forms through the sidewall that is not blocked by the single-sided spacer 42 that is situated adjacent to a neighboring deep trench capacitor. Therefore, there is substantially no out diffusion region between two adjacent trench capacitors. The process window during STI process is increased because the DT-AA misalignment is allowed.

[0034] Please refer to Fig.12. Fig.12 is a top view layout after forming the AA photoresist 90 but before STI etching process in accordance with the third preferred embodiment of the present invention. As shown in Fig.12, the AA photoresist 90 is a strap across two adjacent deep trenches. A portion of the single-sided spacer 42 that is masked by the AA photoresist 90 serves as isolation dielectric between two adjacent trench capacitors.

[0035] Those skilled in the art will readily observe that numerous modifications and alterations of the present invention method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the

appended claims.